IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A memory device comprising:

a plurality of banks, each bank including a plurality of memory core blocks that are selected for activation or deactivation together, the memory core blocks arranged in a plurality of first strips and second strips, the second strips orthogonal to the first strips, a first one of the first strips including a all memory core blocks from a first memory bank and all memory core blocks from a second memory bank, the memory core blocks from the first and second banks being interleaved in the first one of the first strips row in an alternating fashion; and

a plurality of sense amplifiers shared between and interleaved, in the first one of the first strips, with the memory core blocks of the first and second memory banks.

2. (Previously Presented) The memory device of claim 1 wherein column decode conductors traverse the memory core blocks in the first one of the first strips.

3. (Original) The memory device of claim 2 further comprising sense nodes substantially parallel to the column decode conductors.

4. (Previously Presented) The memory device of claim 1 wherein each one of the first strips interleaves all memory core blocks from two different banks.

5. (Previously Presented) A memory device comprising:

a plurality of memory cores logically arranged into a plurality of banks, each bank selectably activating or deactivating its memory cores together as a group, with each memory core assigned to a unique one of the memory banks, and the memory cores are arranged into a plurality of first strips and second strips, wherein the second strips are orthogonal to the first strips, and with each memory core in a first one of the second strips being associated with a different one of the banks;

a plurality of sense amplifiers, each sense amplifier being shared between two unique memory cores in a first one of the first strips, wherein the two unique memory cores are from different banks; and

wherein the memory cores in a first one of the first strips are arranged in an alternating fashion of two different banks with a sense amplifier between adjacent memory cores in the first one of the first strips.

6. (Previously Presented) The memory device of claim 5 further comprising column decode conductors for the first one of the first strips, the column decode conductors for the first one of the first strips being coupled to all the sense amplifiers in the first one of the first strips.

7. (Previously Presented) The memory device of claim 5 wherein the first one of the first strips includes all memory cores from a first one of the banks.

8. (Previously Presented) The memory device of claim 5 wherein the first one of the first strips includes all memory cores from a first one of the banks and all memory cores from a second one of the banks.

9. (Previously Presented) A memory device comprising:

a first bank of memory cores arranged in a linear strip and selectable for activation and deactivation together as a first group;

a second bank of memory cores interleaved in the linear strip with memory cores of the first bank, the second bank of memory cores selectable for activation and deactivation together as a second group; and

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank along the linear strip, the strip comprising only those memory cores from the first and second banks.

10. (Previously Presented) The memory device of claim 9 further comprising a plurality of memory cores arranged as horizontal strips and a plurality of memory cores of vertical strips

arranged perpendicular to the horizontal strips, wherein the linear strip is one of the plurality of horizontal strips.

11. (Previously Presented) The memory device of claim 10 wherein each of the plurality of horizontal strips includes interleaved memory cores from two different banks.

12. (Original) The memory device of claim 9 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

13. (Canceled)

14. (Previously Presented) A memory device comprising:

a first bank of memory cores arranged in a strip that includes all of the memory cores in the first bank, the first bank of memory cores selectable for activation and deactivation together as a first group;

a second bank of memory cores interleaved with the first bank of memory cores arranged in the strip that includes all of the memory cores in the second bank, the second bank of memory cores selectable for activation and deactivation together as a second group independently from the first group;

a plurality of sense amplifiers shared between memory cores of the first bank and memory cores of the second bank; and

a column decoder arranged to drive column decode lines coupled to the plurality of sense amplifiers.

15. (Previously Presented) The memory device of claim 14 further comprising a plurality of memory cores arranged in horizontal strips and a plurality of memory cores arranged in vertical strips arranged perpendicular to the horizontal strips, wherein the strip is one of the plurality of horizontal strips.

16. (Previously Presented) The memory device of claim 15 wherein each of the plurality of horizontal strips includes interleaved memory cores from only two different banks.

17. (Original) The memory device of claim 14 wherein each of the plurality of sense amplifiers is coupled to one memory core of the first bank and one memory core of the second bank.

18. (Previously Presented) An integrated circuit comprising:

an array of memory cores arranged as rows along a first dimension and arranged as columns along a second dimension; and

wherein a strip of memory cores in the first dimension includes all of the memory cores from a first bank interleaved with all of the memory cores from a second bank interspersed with shared sense amplifiers between memory cores of different banks, wherein each particular bank is selectable to activate or deactive all of the memory cores associated with the particular bank.

19. (Previously Presented) The integrated circuit of claim 18 wherein the first dimension includes a plurality of horizontal strips of memory cores, and the second dimension includes a plurality of vertical strips of memory cores, and each of the plurality of horizontal strips includes interleaved memory cores from two different banks.

20. (Previously Presented) The integrated circuit of claim 19 wherein each of the plurality of vertical strips includes non-interleaved memory cores from different banks, and each memory core in a particular vertical strip is from a different bank than the other memory cores in that same particular vertical strip.

21. (Original) The integrated circuit of claim 18 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder and situated substantially parallel to the strip of memory cores.

22. (Previously Presented) An integrated circuit comprising:

an array of memory cores, the array having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes all of the memory cores from a first bank interleaved with all of the memory cores from a second bank, wherein each bank is selectable to activate or deactivate all of the memory cores in that bank; and

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank.

23. (Previously Presented) The integrated circuit of claim 22 wherein:

the first dimension includes a plurality of horizontal strips of memory cores;

the second dimension includes a plurality of vertical strips of memory cores; and

each of the plurality of horizontal strips interleaves all of the memory cores from two different banks.

24. (Previously Presented) The integrated circuit of claim 23 wherein each of the plurality of vertical strips includes non-interleaved memory cores, and in which each of the non-interleaved memory cores within a particular vertical strip is associated with a different memory bank.

25. (Original) The integrated circuit of claim 22 further comprising:

a column decoder; and

a plurality of column decode conductors driven by the column decoder, coupled to the plurality of sense amplifiers, and situated substantially parallel to the strip of memory cores.

26. (Previously Presented) An integrated circuit comprising:

an array of memory cores having a first dimension and a second dimension, wherein a strip of memory cores in the first dimension includes memory cores from a first bank interleaved with memory cores from a second bank, and in which the strip includes all of the memory cores in the first bank and all of the memory cores in the second bank, an in which each bank is selectable to activate or deactivate all of its memory cores;

a plurality of sense amplifiers arranged between memory cores from the first bank and memory cores from the second bank; and

column decode conductors coupled to the plurality of sense amplifiers, the column decode conductors arranged to be near memory cores of the first and second bank.

27. (Previously Presented) The integrated circuit of claim 26 wherein the first dimension includes a plurality of horizontal strips of memory cores, and the second dimension includes a plurality of vertical strips of memory cores, and each of the plurality of horizontal strips interleaves all of the memory cores from two different banks.

28. (Previously Presented) The integrated circuit of claim 27 wherein in each of the plurality of vertical strips, each memory core is from a different bank.

29. (Previously Presented) A memory device comprising:

a first bank of memory cores that are selectable together as a first group for activation or deactivation;

a second bank of memory cores that are selectable together as a second group for activation or deactivation; and

a plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores;

wherein all of the memory cores in the first bank and all of the memory cores in the second bank are interleaved in a first horizontal strip on the memory device.

30. (Previously Presented) The memory device of claim 29 further comprising:

a plurality of horizontal strips of which the first horizontal strip is one; and

a plurality of vertical strips of memory cores, each of the plurality of vertical strips of memory cores having non-interleaved memory cores from a plurality of banks.

31. (Previously Presented) The memory device of claim 29 further comprising:

a third bank of memory cores;

a fourth bank of memory cores;

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores; and

wherein the third bank of memory cores and the fourth bank of memory cores are interleaved in a second horizontal strip parallel to the first horizontal strip.

32. (Original) The memory device of claim 29 further comprising pass transistors coupled to the plurality of sense amplifiers to select data from either the first bank of memory cores or the second bank of memory cores.

33. (Previously Presented) A memory device comprising:

a first bank of memory cores that are selectable together as a first group for activation or deactivation;

a second bank of memory cores that are selectable together as a second group for activation or deactivation, wherein all of the memory cores of the first bank and all of the memory cores of the second bank are interleaved in a first horizontal strip on the memory device;

a plurality of sense amplifiers shared between the first bank of cores and the second bank of cores;

a column decoder; and

a plurality of column decode conductors coupled to the column decoder and the plurality of sense amplifiers, the plurality of column decode conductors being substantially parallel to the first horizontal strip on the memory device.

34. (Previously Presented) The memory device of claim 33 further comprising:

a plurality of horizontal strips of which the first horizontal strip is one; and

a plurality of vertical strips of memory cores, each of the memory cores in a particular one of the vertical strips associated with a different bank than the other memory cores in the particular one of the vertical strips.

35. (Previously Presented) The memory device of claim 33 further comprising:

a third bank of memory cores;

a fourth bank of memory cores; and

a plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores;

wherein all of the memory cores in the third bank of memory cores and all of the memory cores in the fourth bank of memory cores are interleaved in a second horizontal strip parallel to the first horizontal strip.

36. (Previously Presented) A memory device comprising:

a plurality of memory cores physically arranged in horizontal strips and vertical strips and logically arranged into banks that share sense amplifiers, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, and wherein all of the memory cores arranged in a first horizontal strip alternate between a first bank and a second bank.

37. (Original) The memory device of claim 36 further comprising:

a column decoder;

column decode conductors coupled between the column decoder and the sense amplifiers shared between the first bank and the second bank; and

sense nodes coupled to the sense amplifiers, arranged substantially parallel to the column decode conductors.

38. (Previously Presented) The memory device of claim 36 wherein all of the memory cores in a second horizontal strip are arranged to alternate between a third bank and a fourth bank.

39. (Previously Presented) The integrated circuit of claim 36 wherein each of the of vertical strips includes non-interleaved memory cores from different banks.

40. (Previously Presented) A memory device comprising:

a plurality of memory cores physically arranged in horizontal strips and vertical strips and logically arranged into banks that share sense amplifiers, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, and wherein all of the memory cores arranged in a first horizontal strip alternate between a first bank and a second bank; and

column decode conductors arranged in the first horizontal strip to cross memory cores from only the first bank and the second bank.

41. (Previously Presented) The memory device of claim 40 further comprising:

a second horizontal strip having interleaved all of the memory cores from a third bank and a fourth bank; and

a second plurality of sense amplifiers shared between the third bank and the fourth bank.

42. (Previously Presented) The memory device of claim 40 wherein each of the vertical strips includes non-interleaved memory cores that are taken only from different banks.

43. (Previously Presented) A memory device comprising:

a plurality of memory cores physically arranged in a plurality of horizontal strips and a plurality of vertical strips and logically arranged into banks, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank; and

wherein each horizontal strip interleaves in alternating fashion all memory cores from only two of the banks, and no two memory cores in any particular vertical strip is from the same bank.

44. (Previously Presented) The memory device of claim 43 further comprising sense amplifiers shared between memory cores in each of the plurality of horizontal strips.

45. (Previously Presented) The memory device of claim 44 further comprising column decode conductors dedicated to each horizontal strip, each column decoder conductor passing over memory cores of two banks and no more.

46. (Previously Presented) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a plurality of horizontal strips and vertical strips of memory cores; and

a plurality of sense amplifiers positioned between memory cores within each horizontal strip, wherein every memory core is associated with a particular bank that is selectable to activate or deactivate all of the memory cores associated with that particular bank, and wherein only every other memory core within a first horizontal strip is assigned to a the same bank, and wherein each of the memory cores in the first horizontal strip are associated with one of only two of the banks, and in which two of the banks are represented by memory cores in the first horizontal strip.

47. (Original) The computer system of claim 46 wherein each sense amplifier is shared between two banks.

48. (Original) The computer system of claim 46 further comprising a memory controller coupled to the processor and the memory device.

49. (Previously Presented) A computer system comprising:

a processor; and

a memory device coupled to the processor, the memory device including:

a first bank of memory cores arranged in a first horizontal strip, wherein the memory cores of first bank are selectable together as a first group for activation or deactivation;

a second bank of memory cores interleaved with the first bank of memory cores in the first horizontal strip, wherein the memory cores of second bank are selectable together as a

second group for activation or deactivation, and wherein all of the memory cores in the first and second banks are located in the first horizontal strip;

a third bank of memory cores arranged in a second horizontal strip, wherein the memory cores of third bank are selectable together as a third group for activation or deactivation; and

a fourth bank of memory cores interleaved with the third bank of memory cores in the second horizontal strip, wherein the memory cores of fourth bank are selectable together as a fourth group for activation or deactivation, and wherein all of the memory cores in the third and fourth banks are located in the second horizontal strip.

50. (Original) The computer system of claim 49 wherein the memory device further includes:

a first plurality of sense amplifiers shared between the first bank of memory cores and the second bank of memory cores; and

a second plurality of sense amplifiers shared between the third bank of memory cores and the fourth bank of memory cores.

51. (Original) The computer system of claim 49 further comprising a memory controller coupled to the processor and the memory device.

52. (Previously Presented) A computer system comprising:

a processor; and

a memory coupled to the processor, the memory including:

a plurality of sense amplifiers;

a first bank of memory cores, each coupled to at least one of the plurality of sense amplifiers, wherein the memory cores of first bank are selectable together as a first group for activation or deactivation; and

a second bank of memory cores, each coupled to at least one of the plurality of sense amplifiers, wherein the memory cores of second bank are selectable together as a second group for activation or deactivation;

wherein all of the memory cores of the first bank and all of the memory cores of the second bank are arranged in a strip with the plurality of sense amplifiers.

53. (Original) The computer system of claim 52 wherein the memory further includes:
column decode conductors coupled to the plurality of sense amplifiers and
a column decoder to drive the column decode conductors.

54. (Original) The computer system of claim 52 further comprising a memory controller coupled to the processor and the memory device.

55. (Previously Presented) A computer system comprising:
a processor;
a memory controller coupled to the processor; and
a memory device coupled to the memory controller, the memory device including:
a plurality of memory cores logically arranged into Rambus-compatible banks, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, and physically arranged into horizontal strips and vertical strips, wherein each vertical strip interleaves all of the memory cores from two different Rambus-compatible banks.

56. (Previously Presented) The computer system of claim 55 wherein the memory device includes sense amplifiers shared between memory cores of Rambus-compatible banks in each horizontal strip.

57. (Previously Presented) A multibank memory device allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, the memory device comprising:
a plurality of memory banks, each memory bank including a plurality of memory cores, the memory cores arranged in strips of comprising horizontal strips and vertical strips, wherein

each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank;

a plurality of sense amplifiers shared among the memory cores of different ones of the plurality of memory banks;

a plurality of column decoders, each column decoder exclusively accessing a horizontal strip of all of the memory cores from only two of the memory banks wherein the memory cores are separated from each other in the horizontal strip by shared sense amplifiers whereby the memory cores of the horizontal strip alternate between the two memory banks.

58. (Previously Presented) A memory architecture having n memory banks which allows simultaneous access of some of the memory banks, each memory bank including a plurality of memory cores, wherein each particular bank is selectable to activate or deactivate all of the memory cores associated with that particular bank, the memory cores arranged in horizontal strips, each horizontal strip having an associated column decoder connected to each memory core of the horizontal strip and each core of the horizontal strip associated with only one of only two memory banks.

59. (Previously Presented) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, the memory architecture comprising:

a plurality of memory banks, each memory bank containing a plurality of memory cores, wherein each bank is selectable to activate or deactivate all of its associated memory cores, the memory cores arranged in strips, each strip containing all memory cores of only two memory banks and the strip having cores arranged to be alternating between the two memory banks with sense amplifiers shared between the cores of the two memory banks.

60. (Previously Presented) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks, the memory architecture comprising a horizontal strip of all of the memory cores from only two of the memory banks interspersed between shared sense amplifiers, each memory core being a part of one of N memory banks, wherein each bank is

selectable to activate or deactivate all of its associated memory cores, the strip having the memory cores laid out so that no two memory cores of the same memory bank share a common sense amplifier.